What is claimed is:

1. An electronic device, comprising

   a. a substrate, having a top surface and a bottom surface;

   b. a buried layer near the top surface, doped with dopant of a first polarity, electrically communicable to a drain terminal;

   c. a body region, having a second top surface, a second bottom surface and a second side surface;

   d. a portion of the body region, having doped with dopant of a second polarity, contacting a gate region communicable to a gate terminal;

   e. a substantially uniformly doped channel region in the body region, having a third top surface, a third bottom surface, and a third side surface communicable to the portion of the body region in d., the third bottom surface being substantially coplanar to the second bottom surfaces and contacting the buried layer, the third top surface being substantially coplanar to the second top surface and contacting a source region; and

   f. the source region, projecting upward from the channel region, electrically communicable to a source terminal.

2. The electronic device in claim 1 in which the substrate is a semiconductor material.

3. The electronic device in claim 2 in which the semiconductor material is p-type silicon.

4. The electronic device in claim 1 in which the buried layer is n-type silicon material communicable to a drain terminal near the top surface through a sinker.

5. The electronic device in claim 1 in which the body region comprises two layers of substantially mono-crystalline n-type silicon layers.

6. The electronic device in claim 1 in which a portion of the body region distant from the second top surface contacts a dielectric region.

7. The electronic device in claim 6 in which the dielectric region comprises a silicon dioxide region formed with a STI technique.

8. The electronic device in claim 1 in which the gate region is substantially p-type polycrystalline silicon.

9. The electronic device in claim 1, in which an electrical current flows in the channel region upon a voltage bias being applied between the source terminal and the drain terminal.

10. The electronic device in claim 9, in which the electrical current flows in a direction substantially perpendicular the top surface of the substrate.

11. The electronic device in claim 9, in which the magnitude of the current is a function of a voltage at the gate terminal.

12. The electronic device in claim 1, in which the channel region is doped with n-type dopant.

13. The electronic device in claim 1, in which the channel region is doped with p-type dopant.

14. A semiconductor integrated circuit device, comprising

a. a semiconductor substrate, having a top surface and a bottom surface;

b. a first layer of semiconductor material near the top surface, doped with a dopant of a first polarity, electrically communicable to a drain terminal near the top surface;

c. a mono-crystalline first region, having a top surface, a bottom surface and a side surface, the lower portion of the side surface contacting an electrically insulating region, and the upper portion of the side surface coupling to a gate region communicable to a gate terminal near the top surface of the substrate;

d. a substantially uniformly doped channel region in the first region, doped with dopant of the first polarity, having a top surface, a bottom surface, and a side surface, the top surface being substantially coplanar to the top surface of the first region, the bottom surface being substantially coplanar to the bottom surfaces of the first region and electrically communicable to the buried layer, the side surface coupling the gate region; and

e. a source region, projecting upward from the channel region, having a top surface electrically communicable to a source terminal, a bottom surface electrically communicable to the top surface of the channel region.

15. The electronic device in claim 14, in which an electrical current flows in the channel region upon a voltage bias being applied between the source terminal and the drain terminal.

16. The electronic device in claim 15, in which the electrical current flows in a direction substantially perpendicular the top surface of the substrate.

17. The electronic device in claim 15, in which the magnitude of the current is a function of a voltage at the gate terminal.

18. The electronic device in claim 14, in which the distance between the top surface and the bottom surface of the channel region is about 0.7 micro-meters, in which about 0.5 micro-meter is attributable to a bottom layer and about 0.2 micro-meters is attributable to a top layer.

19. The electronic device in claim 14, in which the dopant of a first polarity is p-type.

20. The electronic device in claim 14, in which the dopant of a first polarity is n-type.

21. An n-channel silicon JFET, comprising

a. a silicon substrate, having a top surface and a bottom surface;

b. a buried layer of mono-crystalline silicon near the top surface, doped with a n-type dopant to a sheet resistance of about 25 ohms per square, the buried layer being electrically communicable to a drain terminal near the top surface of the substrate;

c. a silicon mono-crystalline first region having a top surface, a bottom surface and a side surface, the distance between the top and the bottom surfaces being about 0.7 micrometers, the lower portion of the side surface contacting a silicon dioxide region and the upper portion of the side surface contacting a p-type, poly-crystalline silicon gate region, a portion of the first region is p-type;

d. the silicon gate region being communicable to a gate terminal near the top surface of the substrate;

e. a substantially uniformly doped, n-type channel-region in the first region, having a top surface, a bottom surface, and a side surface, the top surface being substantially coplanar to the top surface of the first region, the bottom surface being substantially coplanar to the bottom surfaces of the first region and electrically communicable to the buried layer, the side surface contacting the p-type portion of the first region;

f. a first n-type, poly-crystalline-silicon-source region, projecting upward from the channel region and the gate region, having a top surface electrically communicable to a source terminal near the top surface of the substrate, a bottom surface electrically communicable to the top surface of the channel region, a side surface in contact with dielectric sidewall spacers;

g. the first n-type, poly-crystalline-silicon-source region in f. being electrically insulated from the first p-type, poly-crystalline-silicon-gate region.

h. the device being operable channeling an electrical current through the channel region upon a voltage bias being applied between the source terminal and the drain terminal; and

i. the electrical current flowing in a direction substantially perpendicular the top surface of the silicon substrate, the magnitude of the electrical current being a function of a voltage at the gate terminal.

22. An method for making an electronic device, comprising

a. providing a semiconductor substrate of a first conductivity, having a top surface and a bottom surface;

b. forming a buried layer of a second conductivity near the top surface;

c. forming a first semiconductor layer over the buried layer, doping the region with dopant of the second conductivity;

d. forming in the first layer insulation regions that isolate an island of the first-layer material, the insulation regions having substantially the same thickness as the first layer so the insulation regions reaches the buried layer;

e. forming a second semiconductor layer of the second conductivity over the first semiconductor layer and the insulation regions, portions of the second layer bordering the insulation regions being polycrystalline, portions of the second layer bordering the first layer being mono-crystalline;

f. selectively doping the polycrystalline portions of the second layer with dopant of the first polarity;

g. forming a dielectric layer over a portion of the second layer;

h. forming a third semiconductor layer of the second conductivity over the dielectric layer;

i. removing a portion of the third semiconductor layer to form a source structure and a portion of the second semiconductor layer to form a gate structure; and

j. implanting dopant of the first conductivity into the gate structure and dopant of the second conductivity into the source structure.

23. The method in claim 22 in which the semiconductor substrate is silicon.

24. The method in claim 22 in which the insulation regions comprise silicon dioxide formed with a STI technique.

25. The method in claim 22 in which the first semiconductor layer is about 0.5 micrometers thick and the second semiconductor layer is about 0.2 micrometers thick.

26. The method in claim 22 in which the dielectric layer comprises silicon dioxide and silicon nitride.

27. The method in claim 22 in which a portion of the dopant implanted into the gate structure diffuses into the mono-crystalline portion of the second semiconductor layer and the first semiconductor layer.

28. The method in claim 22 in which the first conductivity is p-type.

29. The method in claim 22 in which the first conductivity is n-type.

30. A method for making an n-channel silicon JFET, comprising

a. providing a p-type silicon substrate, having a top surface and a bottom surface;

b. forming a buried layer of mono-crystalline silicon near the top surface, doped with a n-type dopant to a sheet resistance of about 25 ohms per square;

c. forming a 0.5 micrometers silicon mono-crystalline first layer over the buried layer, doping the region with n-type dopant to a concentration of about $1x10^{15}$ dopant ions per cubic centimeter;

d. forming in the first layer insulation regions that isolate islands of the first-layer material, the insulation regions having substantially the same thickness as the first layer so the insulation regions contact the buried layer;

e. forming a 0.2 micrometer silicon second layer over the first layer and the insulation regions, portions of the second layer contacting the insulation regions being polycrystalline silicon, portions of the second layer contacting the first layer being mono-crystalline silicon, doping the second layer with p-type dopant to a concentration of about $1x10^{15}$ dopant ions per cubic centimeter;

f. providing a photoresist pattern uncovering portions of the polycrystalline silicon;

g. implanting into portions of the polycrystalline silicon uncovered by the photoresist pattern with p-type dopant ions;

h. forming a dielectric layer of silicon dioxide and silicon nitride over the second layer;

i. patterning and etching the dielectric layer to form a opening region over the second layer free of the dielectric material;

j. forming a third n-type silicon layer over the dielectric layer;

k. removing a portion of the third silicon layer and a portion of the second silicon layer;

l. implanting p-type dopant into the second silicon regions to form a gate structure; and

m. anneal the silicon substrate at a elevated temperature.